# AS5001 Arcadium™ Low Jitter Fixed Frequency Oscillator, 10 kHz to 350 MHz

The AS5001 Arcadium™ all-silicon oscillator utilizes proprietary frequency synthesis and sensor technologies to provide a quartz-free, MEMS-free, low jitter clock at any output frequency. The device is factory-programmed to a fixed frequency ranging from 10 kHz to 350 MHz with < 0.026 ppb resolution and maintains low jitter across its operating range. It uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliabilities even in high impact shock scenarios.

AS5001's on-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched- mode power supplies. Offered in a variety of industry-standard packages, the AS5001 has a dramatically simplified supply chain that enables Aeonsemi to ship samples shortly after receipt of order. The AS5001 is factory-configurable for a wide variety of user specifications, including frequency, output format, and OE pin location. Specific configurations are factory programmed at time of shipment, eliminating the long lead times associated with custom oscillators. This process also guarantees 100% electrical testing of every device before shipment.
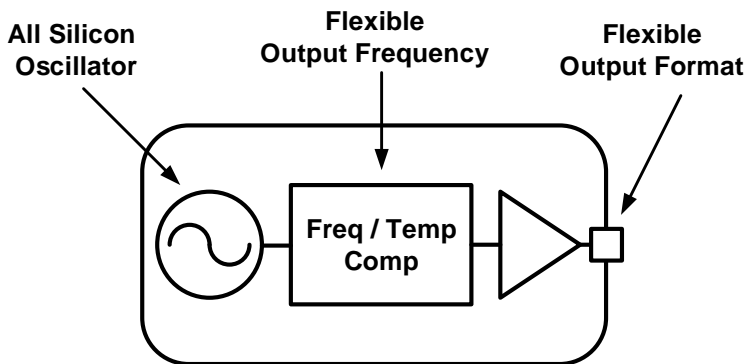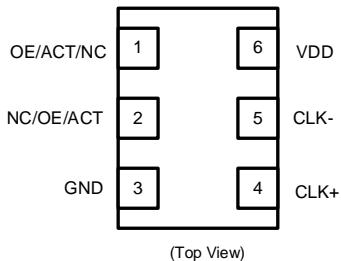
KEY FEATURES

- Quartz-free and MEMS-free without mechanical moving parts
- Available with frequencies from 10 kHz to 350 MHz
    - Differential: 10 kHz to 350 MHz
    - LVCMOS: 10 kHz to 212.5 MHz
- Low jitter: 350 fs Typ RMS (12 kHz – 20 MHz bandwidth)
- Compliant to PCIe Gen 1/2/3/4/5 jitter requirements
- 50 ppm stability (-40 to 105ºC)
- Integrated LDO for on-chip power supply noise filtering
- Support continuous 1.8V to 3.3V V_{DD} supply operation
- LVPECL, LVDS, CML, HCSL, CMOS, and Dual CMOS output options
- Industrial standard 3.2 x 5, 2.5 x 3.2 mm package footprints

APPLICATIONS

- 1G/10G/40G/100G Ethernet
- Servers, switches, storage, NICs, search acceleration
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clocking

All Silicon Oscillator · Flexible Output Frequency · Flexible Output Format — Freq / Temp Comp

Pin Assignments

(LVPECL/LVDS/HCSL/CML/Dual CMOS)

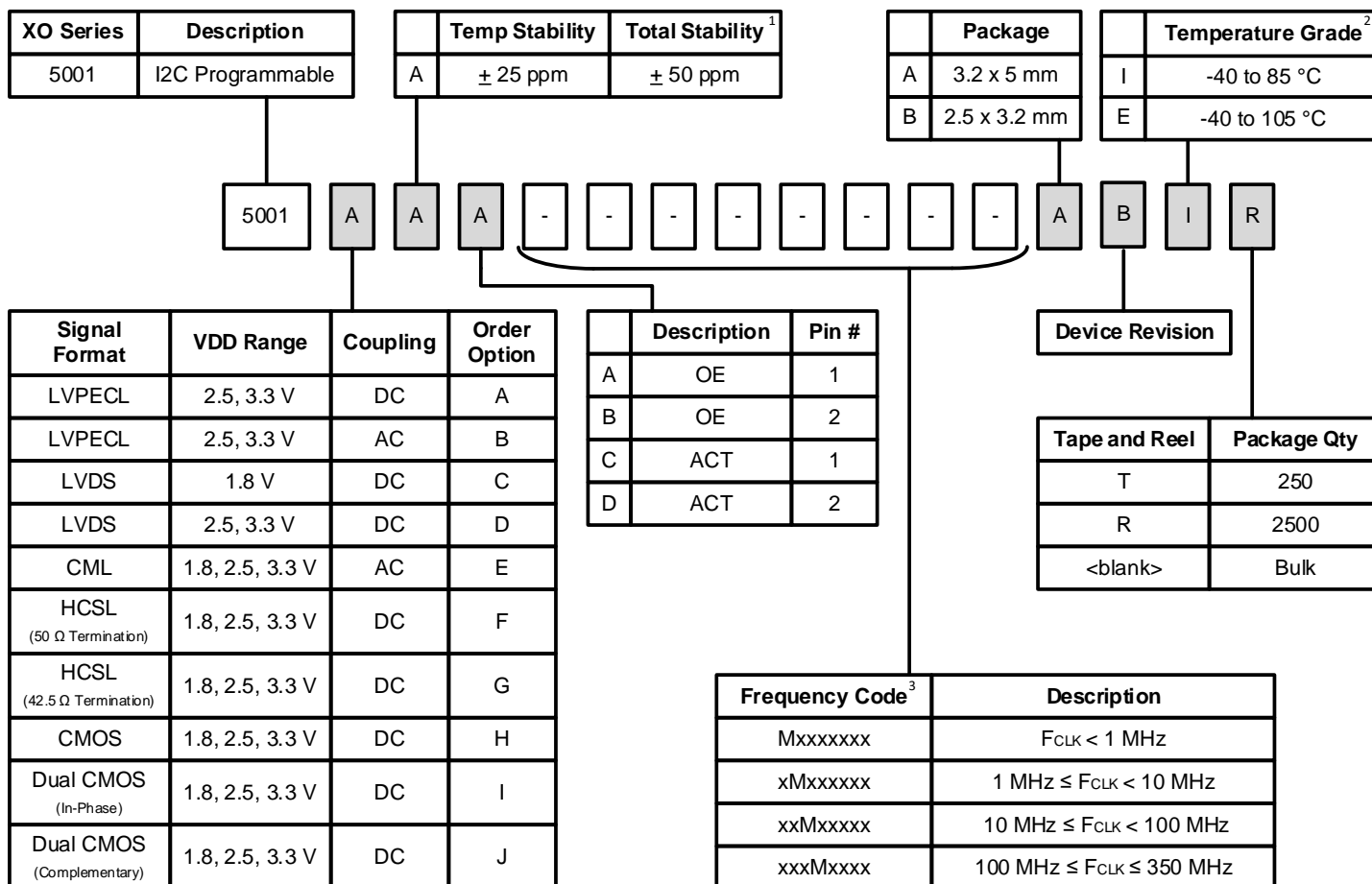| Pin		
OE/ACT/NC	1	6	VDD
NC/OE/ACT	2	5	CLK-
GND	3	4	CLK+

(Top View)

3.2 x 5 mm and 2.5 x 3.2 mm

Pin #	Descriptions
1, 2	*Selectable via ordering option* OE = Output enable. Active High ACT = Device active. Active High NC = No connect
3	GND = Ground
4	CLK+ = Clock output
5	CLK- = Complementary clock output
6	VDD = Power supply

AS5001

1. Ordering Guide

The AS5001 Oscillator supports a variety of options including frequency, output format, and OE/ACT pin location, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 2 weeks.

XO Series	Description
5001	I2C Programmable

	Temp Stability	Total Stability [1]
A	± 25 ppm	± 50 ppm

	Package
A	3.2 x 5 mm
B	2.5 x 3.2 mm

	Temperature Grade [2]
I	-40 to 85 °C
E	-40 to 105 °C

5001	A	A	A	-	-	-	-	-	-	-	-	A	B	I	R

Signal Format	VDD Range	Coupling	Order Option
LVPECL	2.5, 3.3 V	DC	A
LVPECL	2.5, 3.3 V	AC	B
LVDS	1.8 V	DC	C
LVDS	2.5, 3.3 V	DC	D
CML	1.8, 2.5, 3.3 V	AC	E
HCSL (50 Ω Termination)	1.8, 2.5, 3.3 V	DC	F
HCSL (42.5 Ω Termination)	1.8, 2.5, 3.3 V	DC	G
CMOS	1.8, 2.5, 3.3 V	DC	H
Dual CMOS (In-Phase)	1.8, 2.5, 3.3 V	DC	I
Dual CMOS (Complementary)	1.8, 2.5, 3.3 V	DC	J

	Description	Pin #
A	OE	1
B	OE	2
C	ACT	1
D	ACT	2

Device Revision

Tape and Reel	Package Qty
T	250
R	2500
<blank>	Bulk

Frequency Code [3]	Description
Mxxxxxxx	F_{CLK} < 1 MHz
xMxxxxxx	1 MHz ≤ F_{CLK} < 10 MHz
xxMxxxxx	10 MHz ≤ F_{CLK} < 100 MHz
xxxMxxxx	100 MHz ≤ F_{CLK} ≤ 350 MHz

Notes:

1. Total stability includes temp stability, initial accuracy, load pulling, V_{DD} variation, and 10 years aging at 40 °C.

2. Device supports extended industrial temperature range of -40 to 105°C only with V_{DD} = 1.8V (+/- 5%).

3. For example: 156.25 MHz = 156M250; 25 MHz = 25M0000.

2. Electrical Specifications

Table 2.1. Electrical Specifications

V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = –40 to 85 ºC; V_{DD} = 1.8 V ± 5%, T_A = –40 to 105 ºC

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Temperature Range	T_A		–40	—	105	ºC
Frequency Range	F_{CLK}	LVPECL, LVDS, CML, HCSL	0.01	—	350	MHz
		CMOS, Dual CMOS	0.01	—	212.5	MHz
Supply Voltage	V_{DD}		1.71		3.47	V
Supply Current (F_{CLK} = 50 MHz)	I_{DD}	Tristate Hi-Z (OE = 0, output disabled)	—	40	50	mA
		Ready State (ACT = 0, standby mode)	—	1	2	mA
		LVPECL (DC-Coupled)	—	70	80	mA
		LVPECL (AC-Coupled)	—	60	70	mA
		LVDS	—	45	55	mA
		HCSL	—	60	70	mA
		CML	—	60	70	mA
		CMOS	—	40	55	mA
		Dual CMOS	—	50	60	mA
Total Stability[1]	F_{STAB}	Frequency stability	–50	—	50	ppm
Rise/Fall Time (20% to 80% V_{PP})	T_R/T_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS / Dual CMOS (C_L = 5 pF)	—	0.5	1.5	ns
		HCSL, F_{CLK} >50 MHz	—	—	550	ps
Duty Cycle	D_C	All formats	45	—	55	%
Output Enable (OE)[2]	V_{IH}		0.7 × V_{DD}	—	—	V
	V_{IL}		—	—	0.3 × V_{DD}	V
	T_D	Output Disable Time, F_{CLK} >10 MHz	—	—	3	µs
	T_E	Output Enable Time, F_{CLK} >10 MHz	—	—	20	µs
Powerup Time	t_{OSC}	Time from 0.9 × V_{DD} until output frequency (F_{CLK}) within spec	—	—	4	ms
LVPECL Output Option[3] (DC-Coupled)	V_{OC}	Mid-level	V_{DD} – 1.55	—	V_{DD} – 1.25	V
	V_O	Swing (diff)	1.4	—	1.85	V_{PP}
LVPECL Output Option[3] (AC-Coupled)	V_O	Swing (diff)	1.4	—	1.85	VPP
LVDS Output Option[3] (DC-Coupled)	V_{OC}	Mid-level (2.5 V, 3.3 V VDD)	1.125	1.20	1.275	V
		Mid-level (1.8 V VDD)	0.795	0.85	0.905	V
	V_O	Swing (diff)	0.5	0.82	0.96	V_{PP}

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
HCSL Output Option[5] (R_{term} = 50 Ω; DC-Coupled)	V_{OH}	Output voltage high	695	815	935	mV
	V_{OL}	Output voltage low	0	5	10	mV
HCSL Output Option[5] (R_{term} = 42.5 Ω; DC-Coupled)	V_{OH}	Output voltage high	695	820	945	mV
	V_{OL}	Output voltage low	0	5	10	mV
CML Output Option[4] (AC-Coupled)	V_O	Swing (diff)	0.725	0.8	0.89	V_{PP}
CMOS Output Option	V_{OH}	I_{OH} = 8/6/4 mA for 3.3/2.5/1.8V V_{DD}	0.83 × V_{DD}	—	—	V
	V_{OL}	I_{OL} = 8/6/4 mA for 3.3/2.5/1.8V V_{DD}	—	—	0.17 × V_{DD}	V

Notes:

1. Total Stability includes temperature stability, initial accuracy, load pulling, V_{DD} variation, and aging for 10 years at 40ºC.
2. OE includes a 50 kΩ pull-up to VDD for OE active high. Includes a 50 kΩ pull-down to GND for OE active low. NC (No Connect) pins include a 50 kΩ pull-down to GND.
3. R_{term} = 50 Ω to V_{DD} – 2.0 V (see Figure 4.1).
4. R_{term} = 100 Ω (differential) (see Figure 4.2).
5. R_{term} = 50 Ω to GND (see Figure 4.2).

Table 2.2. Clock Output Phase Jitter and PSRR

V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = –40 to 85 ºC; V_{DD} = 1.8 V ± 5%, T_A = –40 to 105 ºC

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Phase Jitter (RMS, 12 kHz - 20 MHz)[1,2] F_{CLK} ≥ 10 MHz	ϕ_J	Differential Formats	—	350	750	fs
		CMOS, Dual CMOS	—	350	—	fs
Phase Jitter (RMS, 50 kHz - 20 MHz) F_{CLK} ≥ 156.25 MHz	ϕ_J	Differential Formats	—	150	250	fs
		CMOS, Dual CMOS	—	100	—	fs
Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output V_{DD} = 1.8 V	PSRR	100 kHz sine wave	—	-76	—	dBc
		200 kHz sine wave	—	-75	—	
		500 kHz sine wave	—	-75	—	
		1 MHz sine wave	—	-75	—	
Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output V_{DD} = 2.5 or 3.3 V	PSRR	100 kHz sine wave	—	-83	—	dBc
		200 kHz sine wave	—	-83	—	
		500 kHz sine wave	—	-83	—	
		1 MHz sine wave	—	-82	—	

Note:
1. Applies to output frequency: 50, 100, 156.25, 212.5, 350 MHz
2. Guaranteed by characterization. Jitter inclusive of any spurs

Figure 2.1: Phase Noise at 156.25 MHz
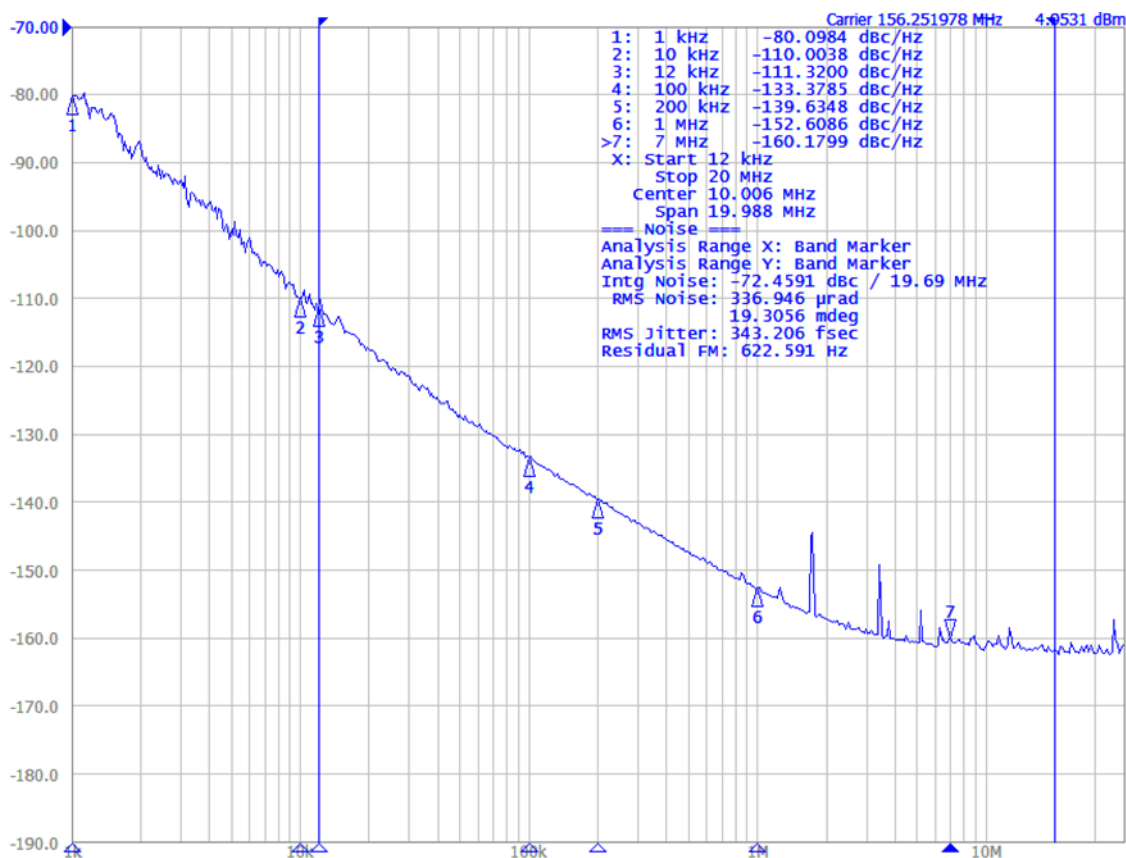
Table 2.3. Environmental Compliance and Package Information

Parameter	Test Condition
Moisture Sensitivity Level	1

Note:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact-us/

Table 2.4. Thermal Conditions

Package	Parameter	Symbol	Test Condition	Value	Unit
3.2 x 5 mm, 6-pin DFN	Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	105	ºC/W
	Thermal Resistance Junction to Board	Θ_{JB}	Still Air	81	ºC/W
	Max Junction Temperature	T_J	Still Air	125	ºC
2.5 x 3.2 mm, 6-pin DFN	Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	108	ºC/W
	Thermal Resistance Junction to Board	Θ_{JB}	Still Air	84	ºC/W
	Max Junction Temperature	T_J	Still Air	125	ºC

Table 2.5. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum Operating Temperature[2]	T_{AMAX}	105	ºC
Storage Temperature	T_S	-55 to 125	ºC
Supply Voltage	V_{DD}	-0.5 to 3.8	V
Input Voltage	V_{IN}	-0.5 to V_{DD} + 0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
Solder Temperature[3]	T_{PEAK}	260	ºC
Solder Time at T_{PEAK}[3]	T_P	20 - 40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. For V_{DD} = 1.8V only; otherwise 85ºC.

3. The device is compliant with JEDEC J-STD-020.

3. CMOS Buffer and Output Terminations

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single AS5001 device.
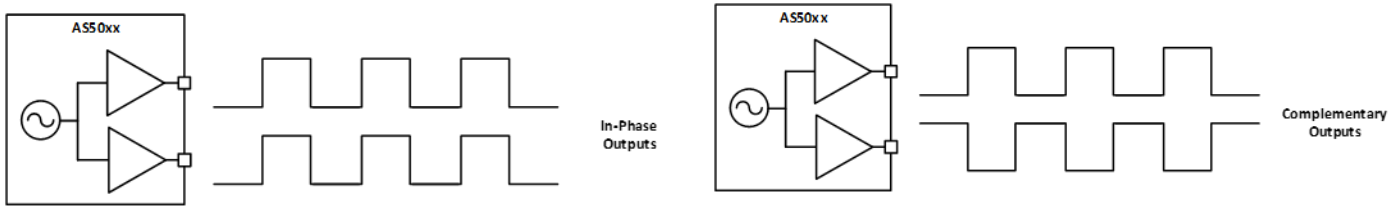

Figure Error! No text of specified style in document.**.1: Integrated 1:2 CMOS Buffer Supports In-Phase or Complementary Outputs**
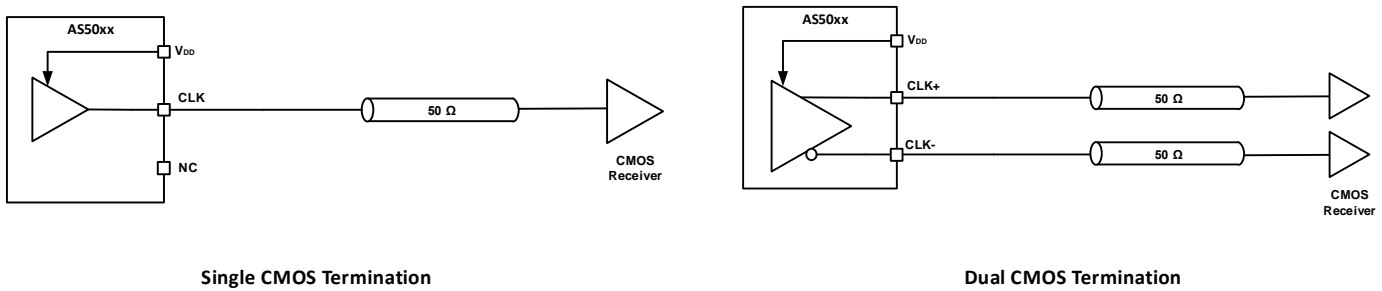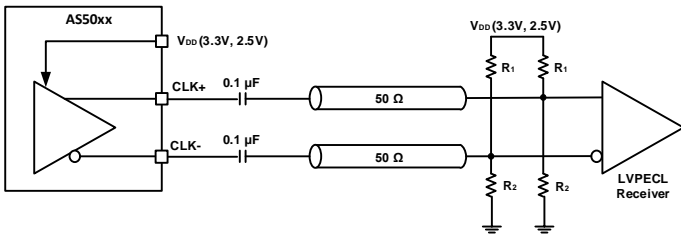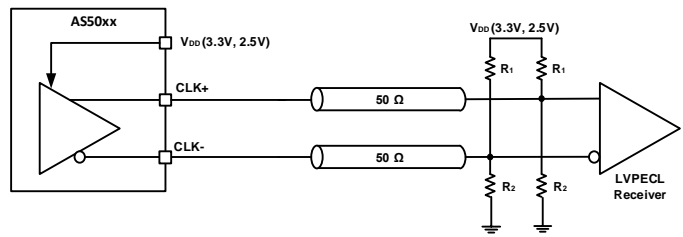

Figure Error! No text of specified style in document.**.2:   CMOS Output Terminations**

4. Recommended Output Terminations

The output drivers support AC-coupled or DC-coupled terminations as shown in figures below.

AC-Coupled LVPECL – Thevenin Termination

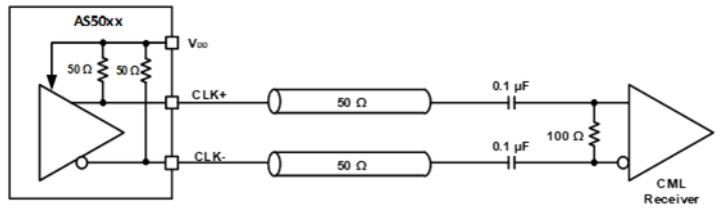**DC-Coupled LVPECL – 50 Ω w/ VTT Bias**
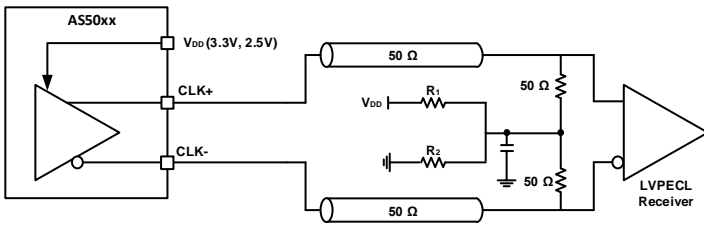
DC-Coupled LVPECL – Thevenin Termination
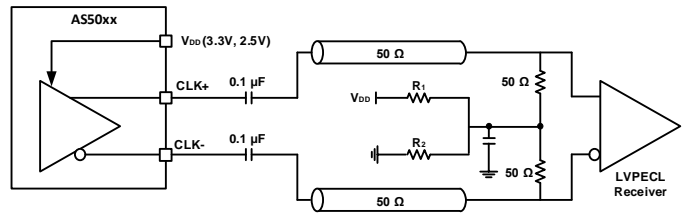
AC-Coupled LVPECL – 50 Ω w/ VTT Bias

Termination Resistor Values		
V_{DD}	R1	R2
3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω

Figure Error! No text of specified style in document.**.3: LVPECL Output Terminations**
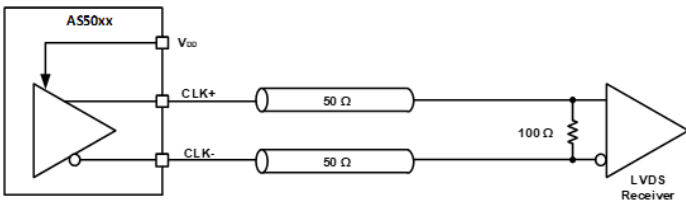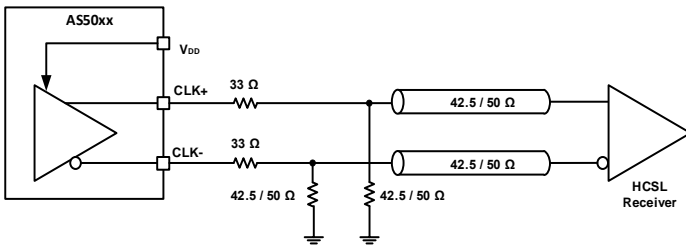
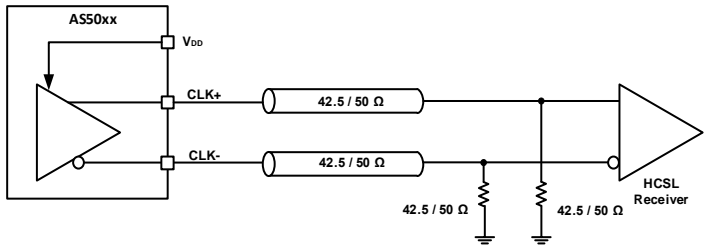DC-Coupled LVDS   AC-Coupled CML

Figure Error! No text of specified style in document.**.4: LVDS / CML Output Terminations**

Source Terminated HCSL   Destination Terminated HCSL

Figure Error! No text of specified style in document.**.5: HCSL Output Terminations**

5. Package Outline

5.1 Package Outline (3.2 x 5 mm)

The figure below illustrates the package details for the 3.2 x 5 mm AS5001. The table below lists the values for the dimensions shown in the illustration.
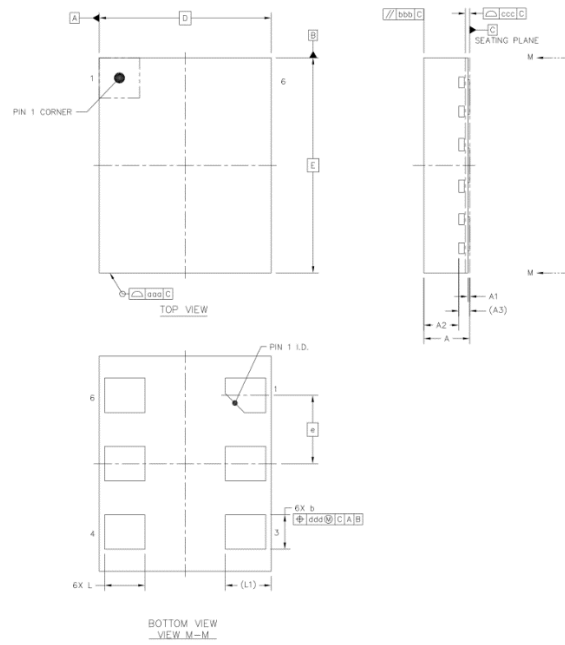

Figure 5.1. AS5001 (3.2 x 5 mm) Outline Diagram

Table 5.1. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	--	0.65	--
A3	0.203 REF		
b	0.59	0.64	0.69
D	3.2 BSC		
E	4 BSC		
e	1.27 BSC		
L	0.7	0.75	0.8
L1	0.85 REF		
aaa	0.1		
bbb	0.1		
ccc	0.08		
ddd	0.1		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

5.2 Package Outline (2.5 x 3.2 mm)

The figure below illustrates the package details for the 2.5 x 3.2 mm AS5001. The table below lists the values for the dimensions shown in the illustration.
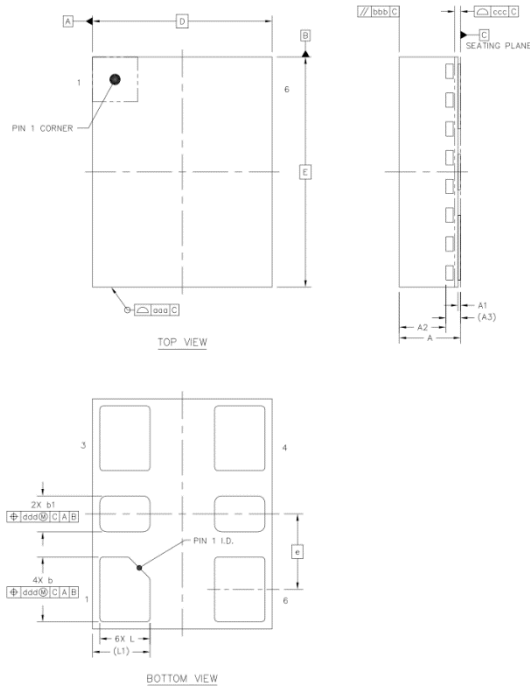

Figure 5.2. AS5001 (2.5 x 3.2 mm) Outline Diagram

Table 5.2. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	---	0.65	---
A3		0.203 REF	
b	0.85	0.9	0.95
b1	0.45	0.5	0.55
D		2.5 BSC	
E		3.2 BSC	
e		1.05 BSC	
L	0.65	0.7	0.75
aaa		0.1	
bbb		0.1	
ccc		0.08	
ddd		0.1	

Notes:

1. The dimensions in parentheses are reference.
2. All dimensions in millimeters (mm).
3. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

6. PCB Land Pattern (3.2 x 5 mm and 2.5 x 3.2 mm)

The figure below illustrates the 3.2 x 5 mm PCB land pattern for the AS5001. The table below lists the values for the dimensions shown in the illustration.
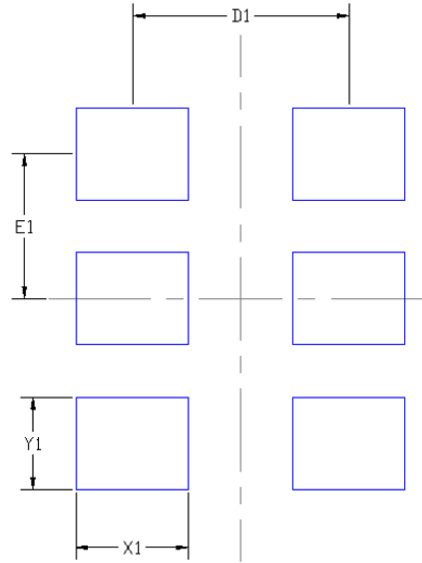

Figure 6.1. AS5001 (3.2 x 5 mm and 2.5 x 3.2 mm) PCB Land Pattern

Table 6.1. PCB Land Pattern Dimensions (mm)

Dimension	Description	3.2 x 5 mm Package Value (mm)	2.5 x 3.2 mm Package Value (mm)
X1	Width - leads on long sides	0.75	0.7
Y1	Height - leads on long sides	0.64	0.9, 0.5
D1	Pitch in X directions of XLY1 leads	2.25	1.6
E1	Lead pitch XLY1 leads	1.27	1.05

Notes: The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8:1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Top Marking (3.2 x 5 mm and 2.5 x 3.2 mm)

The figure below illustrates the mark specification for the AS5001. The table below lists the line information.
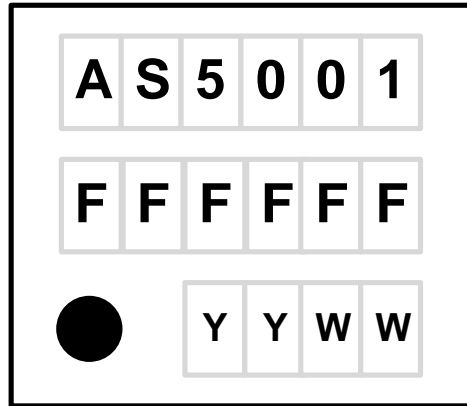

Figure 7.1. AS5001 Top Mark

Table 7.1. AS5001 Top Mark Description

Line	Position	Description
1	1–6	A = AS5001, CCCCC = Custom Mark Code
2		**Trace Code**
	1–6	6 digits trace code per assembly release instructions
3	Position 1	Pin 1 orientation mark (dot)
	Position 2–3	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 4–5	Calendar Work Week number (1–53), to be assigned by assembly site

8. Revision History

Revision 0.9

Sept 2020

- Initial release